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Description

[INTEGRATED CIRCUIT YIELD ENHANCEMENT USING VORONOI DIAGRAMS]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application is related to pending U.S. Patent Application 10/709,293, filed concurrently herewith to Allen et al., entitled "CRITICAL AREA COMPOSITE FAULT MECHANISMS USING VORONOI DIAGRAMS" (IBM Docket No. BUR920030136US1). The foregoing application is assigned to the present assignee, and is incorporated herein by reference.

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BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention generally relates to measuring critical area in integrated circuit design, and more particularly to a method that uses Voronoi diagrams to measure critical area as the design layout is changed.